1. Approving Civil Aviation Authority Country:	2.	3. Form Tracking Number:
FAA/United States	**AUTHORIZED RELEASE CERTIFICATE** FAA Form 8130-3, AIRWORTHINESS APPROVAL TAG	613440-192582-756

4. Organization Name and Address:	5. Work Order/Contract/Invoice Number:
ELDEC Aerospace Corp. 16700 13th Avenue West Lynnwood, WA 98037-8597 (AG4R049M)	WR2551781

6. Item:	7. Description:	8. Part Number:	9. Quantity:	10. Serial Number:	11. Status/Work:
1	PCM	4-949-01 (182533-002)	1	192582-756 (111100756)	Repaired

12. Remarks TSN: N/A CSN: N/A TSO: N/A CSO: N/A

Found left latch binds and found no water damages. Replaced left latch. Testing after inspections and cleaning steps were complete confirmed that no failures are present. Unit was reassembled and passes all inspections and final tests. All work and testing was accomplished in accordance with CMM 42-20-02, Rev 8, Dated May 23, 2019.
Customer PO#: 900334836.

Certifies that the work specified in Block 11/12 was carried out in accordance with EASA Part 145 and in respect to that work the article is considered ready for release to service under EASA Part 145 approval no. EASA 145-5067.

13a. Certifies that items identified above were manufactured in conformity to	14a. ☒ 14 CFR 43.9 Return to Service ☒ Other regulation specified in Block 12
☐ Approved design data and are in a condition for safe operation ☐ Non-approved design data specified in Block 12	Certifies that unless otherwise specified in Block 12, the work identified in Block 11 and described in Block 12 was accomplished in accordance with Title 14, Code of Federal Regulations, part 43, and in respect to that work, the items are approved for return to service.

13b. Authorized Signature:	13c. Approval/Authorization No:	14b. Authorized Signature:	14c. Approval/Certificate No:
			AG4R049M
13d. Name (*Typed or Printed*)	13e. Date (dd/mmm/yyyy)	14d. Name (*Typed or Printed*)	14e. Date (dd/mmm/yyyy):
		Jim Tran	24/AUG/2022

User/Installer Responsibilities

It is important to understand that the existence of this document alone does not automatically constitute authority to install the aircraft engine/propeller/article.
Where the user/installer work in accordance with the national regulations of an airworthiness authority different than the airworthiness authority of the country specified in Block 1 it is essential that the user/installer ensure that his/her airworthiness authority accepts aircraft engine(s)/propeller(s)/article(s) from the airworthiness authority of the country specified in Block 1.
Statements in Blocks 13a and 14a do not constitute installation certification. In all cases, aircraft maintenance records must contain an installation certification issued in accordance with the national regulations by the user/installer before the aircraft may be flown.

1. PART OR MATERIAL CERTIFICATION FORM

ATA Specification 106

2. Seller's Name: GE Aviation Systems

3. Reference # SR259353

4. Organization: GE Aviation Systems
Address: 14100 Roosevelt Blvd.
Clearwater, FL 33762

Phone#: 727-532-6655
FAX #: 727-532-6435
SITA/Wire Code: N/A
Status: FAA Repair Station RI3R816L

5A. Seller's Contract #: N/A

5B. Buyer's Contract #: N/A

6. Item	7. Description	8. Manufacturer & Part #	9. Eligibility	10. Qty	11. Serial/Batch #	12. Status
1	POWER CONDITIONING MODULE (PCM)	182533-002	N/A	1	111100756	REPAIRED

13A. *Remarks*

Refer to FAA Form 8130-3 and Warranty & Repair Strip Report included (RMA Number/Form Tracking Number: 613440-192582-756).
MFG PN: 4-949-01, SN: 192582-756.

13B. Obtained From Eldec Corporation

13C. Last Certificated Agency Eldec Corporation

14. New Parts/Material Verification:

The following signature attests that the part(s) or Material(s) identified above was (were) manufactured by a FAA Production Approval Holder (PAH), or to an industry or commercial standard.

15. Signature

16. Name

17. Date

18. Used, Repaired or Overhauled Parts Verification:

The following signature attests that the documentation specified above or attached is accurate with regard to the item(s) described.

19. Signature [signature] QA 06

20. Name Samija Konakovic
Return to Service Inspector

21. Date 02 Sep 2022

NOTICE: the above signature binds the seller and the SIGNER to the accuracy of the information provided in the Form. Should the information provided in this form contain inaccuracies or misrepresentation, the signer and the SELLER may be liable for damages and be subject to criminal prosecution under state and federal law.

CRANE AEROSPACE & ELECTRONICS

ELDEC Aerospace Corp.

16700 13th Avenue West
Lynnwood,WA 98037-8597

Run Date: Aug 24, 2022 8:38 PM

RMA #
613440-192582-756

WARRANTY & REPAIR STRIP REPORT

Phone# (425)743-8255 (Product Support Admin)
24 AOG # (425) 743-8100

2022/08/24 This document contains Data controlled by the EAR. Diversion or use contrary to U.S. law is prohibited. ECCN: 9E991

RMA NUMBER	PART NUMBER AS RCVD	SERIAL NUMBER AS RCVD	RECEIVED DATE	RECEIVED BY	QTY
613440-192582-756	**4-949-01**	**192582-756**	**Aug 23, 2022**	**268936**	**1**

CUSTOMER	CUSTOMER PN	CUSTOMER S/N	HOURS	AIRCRAFT ID
GE AVIATION US	**182533-002**	**111100756**	**TSN**	

SERVICE RQST#	CYCLES
1092777	**CSN**

DATE OF MFG	CUSTOMER PO	REJECTION REF NO.	FAA 8130 STATUS	FAILURE CLASS	REJ VER?
Nov 1, 2011	**900334836**		**Repaired**	**AGE**	**N**

MOD LEVEL RCVD	MOD LEVEL SHIPPED	SHIPPED PART#	SHIPPED SERIAL #
8	**8**	**4-949-01**	**192582-756**

HISTORY OF UNIT

RMA NUMBER	RECEIVE DATE	CUSTOMER	REJ VER?	PROB TYPE	CUSTOMER PO NUMBER
613440-192582-756	Aug 23, 2022	GE AVIATION US	N	HARDWARE	900334836

CUSTOMER REJECTION DESCRIPTION

CUSTOMER_PROBLEM_TEXT

MMSG 42-00808 LEFT 2 PCM HAS FAILED DURING INSP.FOUND WATER INGESTION COLOUR MARKS. EVAL AND QUOTE TO THE LATEST REV OF CMM.
**** For 4-949 units: Note that Shop MUST include customer s/n in both block 10 of the 8130-3 (under Crane s/n) AND on Strip report in "Customer S/N" field.**
HAVE SHOP STOP WORK AFTER EVALUATION. WE NEED CUSTOMER APPROVAL BEFORE COMPLETING WORK.

TROUBLESHOOTING AND WORK PERFORMED

TROUBLESHOOTING_TEXT

Removal reason stated by the customer was not confirmed. Downloaded NVM. The unit was fully tested and found to have no known failures. Due to CCA inspection, the unit was disassembled and all internal assemblies were inspected: Found left latch binds and found no water damages. Photos taken. Replaced left latch. Testing after inspections and cleaning steps were complete confirmed that no failures are present. Unit was reassembled and passes all inspections and final tests. All work and testing was accomplished in accordance with CMM 42-20-02, Rev 8, Dated May 23, 2019.

CRANE AEROSPACE & ELECTRONICS

ELDEC Aerospace Corp.

16700 13th Avenue West
Lynnwood,WA 98037-8597

Run Date: Aug 24, 2022 8:38 PM

RMA #

613440-192582-756

PARTS USED

Part Number	Description	Quantity Issued
HA61-01	HANDLE, LATCHING	1

UUT Status - PASS

Serial/Batch: 192582-756,

Model Type: 4-949-01, ELDEC ATP4-949-01, Rev. K

Test Time: Wednesday, August 24, 2022 14:48:06

Program Version: 13 [CRC32=87FF1183]

Program Comment:

Test Results

Model Type: 4-949-01, ELDEC ATP4-949-01, Rev. K
Wednesday, August 24, 2022 14:48:07
Program Name: ATP94901AH
Test Duration: 0:37:13

Serial/Batch: 192582-756,
Program Version: 13 [CRC32=87FF1183]
Status: Pass
Operator ID: pthai

Status	Test	Test Description	Min.	Actual	Max.	Units
	2	ATE Test System Setup				
	3	Check fixture Validation				
	28	3.31 EEPROM Programming				
	32	Set Initial Inputs to UUT for this test				
Pass	35	Measure P12V Backup_in (V)	11	11.923	13	Vdc
Pass	53	Measure HB_BUS (V)	27	28.002	29	Vdc
Pass	56	Measure P28V_BUS (V)	27	28.575	29	Vdc
	57	Begin Test				
Pass	64	A.2 Measure P12V Backup_in (V)	-1	-0.0011583	1	Vdc
Pass	71	A.4 Measure HB_BUS (V)	-0.5	0.016801	0.5	Vdc
Pass	74	A.5 Measure P28V_BUS (V)	27.8	27.878	28.2	Vdc
Pass	82	G.1 Log Hardware SN; Retrieved: 111100756	0	1.111e+008	1e+009	Decimal
Pass	83	G.2 Log Hardware PN; Retrieved: 182533-002	1.8253e+005	1.8253e+005	1.8253e+005	Decimal
Pass	84	G.3 Log MOD Number; Retrieved: 08	8	8	9	Decimal
Pass	87	J. Measure P28V_BUS (V)	-0.5	0.044301	0.5	Vdc
Pass	91	K. Measure P12V Backup_in (V)	11	11.927	13	Vdc
Pass	92	L.1 Verify Configuration data is correct	1	1	1	
Pass	93	L.2 Verify the Fault log pointers is all 0xFF	255	255	255	
Pass	94	L.3 Verify the ETI hours register is all 0x00	0	0	0	
Pass	95	L.4 Verify the ETI CRC register is all 0x00	0	0	0	
Pass	96	L.5 Verify Spare Register (1)	0	0	0	
Pass	97	L.5 Verify Spare Register (2)	0	0	0	
Pass	98	L.5 Verify Spare Register (3)	0	0	0	
Pass	105	L.6 Verify Configuration CRC byte 1	25	25	25	
Pass	106	L.6 Verify Configuration CRC byte 2	24	24	24	
	108	3.3 Initial Power-On Tests				
	109	Set Initial Inputs to UUT for this test				
Pass	129	Measure HB_BUS (V)	35.8	35.998	36.2	Vdc
Pass	133	Measure P28V_BUS (V)	20	20.435	21	Vdc
	134	Begin Test				
Pass	139	A.1 Verify No-load P12V5 output	12.2	12.509	12.8	Vdc
Pass	140	A.2 Verify No-Load P12V5 ripple	10	120	200	mVolts
Pass	190	A.3 P12V5 Trans Neg	1	1	1	Bool
Pass	240	A.4 P12V5 Trans Pulse	1	1	1	Bool
Pass	290	A.5 P12V5 Trans Pos	1	1	1	Bool
Pass	291	A.6 Verify No-load P12V_BACKUP_OUT output	11.52	11.941	12.48	Vdc
Pass	293	A.7 Verify No-load P12V_BACKUP_OUT ripple	10	16.94	100	mVolts
Pass	294	A.8 Verify Battery Leakage Current	1	2.2106	7	mA
Pass	298	G.1 Verify RR(0) FPGA Revision	167	167	167	Bool
Pass	299	G.2 Verify RR(4) CV_DIR = LOW	0	0	0	Bool
Pass	300	I.1 Verify RR(0) SWTR_ENABLE = HIGH	1	1	1	Bool
Pass	301	I.2 Verify RR(10) FET_STATUS 0 = HIGH	1	1	1	Bool
Pass	302	I.3 Verify RR(10) FET_STATUS 1 = HIGH	1	1	1	Bool
Pass	303	I.4 Verify RR(10) PBIT_FLT_STS = LOW	0	0	0	Bool
Pass	306	K.1 Verify RR(1) ON_OFF_BATTERY = LOW	0	0	0	Bool
Pass	307	K.2 Verify RR(7) MODULE_PRESENT_0	0	0	0	Bool

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	598	D.3 Verify RR(1) P12V_BACK_LMT = LOW	0	0	0	Bool
Pass	599	D.4 Verify RR(1) HB_LMT = LOW	0	0	0	Bool
Pass	602	F.1 Verify No-load FAN_PWR Voltage	26.68	28.081	29.4	Vdc
Pass	603	F.2 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	604	F.3 Verify RR(3) FAN_CURR_LMT = LOW	0	0	0	Bool
Pass	607	H.1 Verify CV_PWR Voltage	-29.12	-28.093	-26.8	Vdc
Pass	608	H.2 Verify RR(4) CV_INHIBIT_IN = LOW	0	0	0	Bool
Pass	609	H.3 Verify RR(3) FAN_INHIBIT_IN = LOW	0	0	0	Bool
	610	3.5 Low-Line, Full-Load Operation				
	611	Set Initial Inputs to UUT for this test				
Pass	628	Measure HB_BUS (V)	-0.5	0.0097094	0.5	Vdc
Pass	632	Measure P28V_BUS (V)	20.3	20.438	20.7	Vdc
	633	Begin Test				
	639	A. Set all power outputs to MAX LOAD				
	642	B.1 Set P28V_BUS = 18V				
Pass	644	B.1 Measure P28V_BUS	17.8	17.845	18.2	Vdc
Pass	648	E.1 Verify RR(1) P28V_LOCAL_LMT = HIGH	1	1	1	Bool
Pass	649	E.2 Verify Input Current <= 60A	20	56.072	60	Adc
Pass	650	E.3 Verify P12V5 LL, FL	12.2	12.502	12.8	Vdc
Pass	652	E.4 Verify P12V5 Pk-Pk Ripple	10	16.94	200	mVolts
Pass	653	E.5 Verify FAN_PWR Voltage	26.68	27.385	29.4	Vdc
Pass	655	E.6 Verify FAN PWR Pk-Pk Ripple	10	16.94	200	mVolts
Pass	656	E.7 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	657	E.8 Verify RR(3) FAN_CURR_LMT = HIGH	1	1	1	Bool
Pass	663	J.1 Verify CV_PWR Voltage	26.8	27.697	29.12	Vdc
Pass	664	J.2 Verify RR(4) CV_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	665	J.3 Verify RR(4) CV_CURRENT_LMT = HIGH	1	1	1	Bool
Pass	666	J.4 Verify P12V_BACKUP_OUT Voltage	11.52	11.91	12.48	Vdc
Pass	668	J.5 Verify P12V_BACKUP_OUT Pk-PK Ripple	10	16.94	100	mVolts
	669	3.6 Nominal-Line, Full-Load Operation				
	670	Set Initial Inputs to UUT for this test				
Pass	687	Measure HB_BUS (V)	-0.5	0.0048342	0.5	Vdc
	689	Set P28V_BUS = 18V				
Pass	691	Measure P28V_BUS	17.8	17.825	18.2	Vdc
	692	Begin Test				
	699	Set P28V_BUS				
Pass	701	A. Measure P28V_BUS	27.8	27.955	28.2	Vdc
Pass	702	B.1 Verify RR(1) P28V_LOCAL_LMT = HIGH	1	1	1	Bool
Pass	703	B.2 Verify FL Input Current	10	35.008	40.18	Adc
Pass	704	B.3 Verify RR(1) P12V5_LMT = HIGH	1	1	1	Bool
Pass	705	B.4 P12V5 NL, FL	53.5	53.593	53.7	A
Pass	705	B.4 P12V5 NL, FL	12.2	12.501	12.8	Vdc
Pass	707	B.5 Verify P12V5 Pk-Pk Ripple	10	50.82	200	mVolts
Pass	708	B.6 Verify FAN_PWR Voltage	5.5984	5.5984	5.5984	A
Pass	708	B.6 Verify FAN_PWR Voltage	26.68	27.386	29.4	Vdc
Pass	710	B.7 Verify FAN Pk-Pk Ripple	10	94.86	200	mVolts
Pass	711	B.8 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	712	B.9 Verify RR(3) FAN_CURR_LMT = HIGH	1	1	1	Bool
Pass	717	F.1 Verify CV_PWR Voltage	-29.12	-27.695	-26.8	Vdc
Pass	718	F.2 Verify RR(4) CV_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	719	F.3 Verify RR(4) CV_CURRENT_LMT = HIGH	1	1	1	Bool
Pass	720	F.4 Verify P12V_BACKUP_OUT Voltage	0.1198	0.1198	0.1198	A

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	933	G.4 CV_PWR on 5s	4.9	5.06	5.1	Sec
Pass	938	I.1 Verify CV_PWR Voltage -1 to 1 V	-1	-9.269e-006	1	Vdc
Pass	939	I.2 Verify RBW(4) CV_ON_PIN = LOW	0	0	0	Bool
Pass	940	I.3 Verify RR(4) CV_VOLTAGE_LMT = LOW	0	0	0	Bool
Pass	941	I.4 Verify RR(4) CV_CURRENT_LMT = HIGH	1	1	1	Bool
Pass	942	I.5 Verify RR(4) CV_INHIBIT_IN = HIGH	1	1	1	Bool
Pass	945	K.1 Verify (RBW4) CV_ON_PIN = LOW	0	0	0	Bool
Pass	949	N.1 Verify RR(4) CV_POSITION_SHUTDN=0	0	0	0	Bool
Pass	951	P.1 Verify CV_PWR Voltage	-29.12	-27.914	-26.8	Vdc
Pass	954	P.1 Verify CV_PWR Voltage -1 to 1 V	-1	6.09e-007	1	Vdc
Pass	955	P.2 Verify RR(4) CV_POSITION_SHUTDN=1	1	1	1	Bool
Pass	956	P.2 Verify RR(4) CV_POSITION_SHUTDN=0	0	0	0	Bool
Pass	960	R.1 Verify (RBW4) CV_ON_PIN=LOW	0	0	0	Bool
Pass	961	R.2 Verify CV_PWR Voltage -1 to 1 V	-1	3.342e-006	1	Vdc
Pass	964	T.1 Verify CV_PWR Voltage -1 to 1 V	-1	5.057e-006	1	Vdc
Pass	967	V.1 Verify CV_PWR Voltage	-29.12	-27.913	-26.8	Vdc
Pass	969	Y.1 Verify RR(4) CV_TIME_TRIP=1	1	1	1	Bool
Pass	970	Y.1 Verify RR(4) CV_TIME_TRIP=0	0	0	0	Bool
Pass	972	Y.1 Verify RR(4) CV_TIME_TRIP=1	1	1	1	Bool
Pass	973	Y.1 Verify RR(4) CV_TIME_TRIP=0	0	0	0	Bool
	975	3.11 Control Valve ECS Direction				
	976	Set Initial Inputs to UUT for this test				
	987	Set Output loads (various levels)				
Pass	995	Measure HB_BUS (V)	-0.5	0.0081808	0.5	Vdc
	996	Set P28V_BUS				
Pass	998	Measure P28V_BUS	27.8	27.996	28.2	Vdc
	999	Begin Test				
Pass	1007	B.1 Verify RR(4) CV_POS = Binary 11	3	3	3	Bool
Pass	1012	F.1 Verify CV_PWR Voltage	26.8	27.93	29.12	Vdc
Pass	1013	F.2 Verify (RBW4) CV_ON_PIN = HIGH	1	1	1	Bool
Pass	1014	F.3 Verify (RBW4) CV_ON_DIR = HIGH	1	1	1	Bool
Pass	1017	H.1 Verify RR(4) CV_INHIBIT_IN = HIGH	1	1	1	Bool
Pass	1018	H.2 Verify CV_PWR is off	-1	1.4227e-005	1	Vdc
Pass	1019	H.3 Verify (RBW4) CV_ON_PIN = LOW	0	0	0	Bool
Pass	1020	H.4 Verify RR(4) CV_VOLTAGE_LMT = LOW	0	0	0	Bool
Pass	1021	H.5 Verify RR(4) CV_CURR_LMT = HIGH	1	1	1	Bool
Pass	1025	K.1 Verify CV_PWR Voltage	26.8	27.93	29.12	Vdc
Pass	1026	M.1 Verify (RBW4) CV_ON_PIN = High	1	1	1	Bool
Pass	1028	M.1 Verify (RBW4) CV_ON_PIN = LOW	0	0	0	Bool
Pass	1030	O.1 Verify (RBW4) CV_ON_PIN = LOW	0	0	0	Bool
Pass	1031	O.2 Verify RR(4) CV_POS = Binary 10	2	2	2	Bool
	1032	3.12 CV ECS Holding Current				
	1033	Set Initial Inputs to UUT for this test				
Pass	1052	Measure HB_BUS (V)	-0.5	0.0084282	0.5	Vdc
	1053	Set P28V_BUS				
Pass	1055	Measure P28V_BUS	27.8	27.998	28.2	Vdc
	1056	Begin Test				
Pass	1067	B.1 Verify (RBW4) CV_ECS_HOLD = HIGH	1	1	1	Bool
Pass	1069	B.2 Verify CV_PWR Holding current 10 to 20 mA	10	11.837	20	mA
Pass	1072	D.1 Verify (RBW4) CV_ECS_HOLD = LOW	0	0	0	Bool
Pass	1073	D.2 Verify CV_PWR is off	-1	6.188e-006	1	Vdc
Pass	1075	F.1 Verify CV_PWR is off	-1	6.138e-006	1	Vdc

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	1344	H.1 P12V5 overload_current	55	59	65	Adc
Pass	1346	H.2 Verify Power Enable 0 = HIGH	2	3.0902	3.5	Vdc
Pass	1347	H.2 Verify Power Enable 1 = HIGH	2	3.0942	3.5	Vdc
Pass	1348	H.2 Verify Power Enable 2 = HIGH	2	3.0959	3.5	Vdc
Pass	1349	H.2 Verify Power Enable 3 = HIGH	2	3.0937	3.5	Vdc
Pass	1350	H.2 Verify Power Enable 4 = LOW	-0.1	0.018871	0.4	Vdc
Pass	1351	H.2 Verify Power Enable 5 = HIGH	2	3.0949	3.5	Vdc
Pass	1352	H.2 Verify Power Enable 6 = HIGH	2	3.0857	3.5	Vdc
Pass	1353	H.2 Verify Power Enable 7 = LOW	-0.1	0.016625	0.4	Vdc
Pass	1354	H.2 Verify Power Enable 8 = HIGH	2	3.0801	3.5	Vdc
Pass	1355	H.2 Verify Power Enable 9 = HIGH	2	3.0853	3.5	Vdc
Pass	1356	H.2 Verify Power Enable 10 = LOW	-0.1	0.019451	0.4	Vdc
Pass	1357	H.2 Verify Power Enable 11 = LOW	-0.1	0.013874	0.4	Vdc
Pass	1358	H.2 Verify Power Enable 12 = LOW	-0.1	0.018493	0.4	Vdc
Pass	1359	H.2 Verify Power Enable 13 = LOW	-0.1	0.014804	0.4	Vdc
Pass	1360	H.3 Verify RR(8) Power_Enable(9) = LOW	0	0	0	Bool
Pass	1361	H.4 Verify RR(8) Power_Enable(8) = LOW	0	0	0	Bool
Pass	1362	H.5 Verify RR(9) Power_Enable(6) = LOW	0	0	0	Bool
Pass	1363	H.6 Verify RR(9) Power_Enable(5) = LOW	0	0	0	Bool
Pass	1364	H.7 Verify RR(9) Power_Enable(3) = LOW	0	0	0	Bool
Pass	1365	H.8 Verify RR(9) Power_Enable(2) = LOW	0	0	0	Bool
Pass	1366	H.9 Verify RR(9) Power_Enable(1) = LOW	0	0	0	Bool
Pass	1367	H.10 Verify RR(9) Power_Enable(0) = LOW	0	0	0	Bool
Pass	1368	H.11 Verify RR(39) P12V5_OC = HIGH	1	1	1	Bool
Pass	1373	K.1 P12V5 Shutdown Current	57	61.5	68	Adc
Pass	1376	K.2 P28V_BUS Current	0.19934	0.882	1.1993	Adc
Pass	1377	K.3 Verify (RBW4) SWTR_ENABLE = LOW	0	0	0	Bool
Pass	1379	K.4 Verify Power Enable 0 = HIGH	2	3.1481	3.5	Vdc
Pass	1380	K.4 Verify Power Enable 1 = HIGH	2	3.125	3.5	Vdc
Pass	1381	K.4 Verify Power Enable 2 = HIGH	2	3.126	3.5	Vdc
Pass	1382	K.4 Verify Power Enable 3 = HIGH	2	3.1239	3.5	Vdc
Pass	1383	K.4 Verify Power Enable 4 = HIGH	2	3.1217	3.5	Vdc
Pass	1384	K.4 Verify Power Enable 5 = HIGH	2	3.1248	3.5	Vdc
Pass	1385	K.4 Verify Power Enable 6 = HIGH	2	3.1144	3.5	Vdc
Pass	1386	K.4 Verify Power Enable 7 = HIGH	2	3.1201	3.5	Vdc
Pass	1387	K.4 Verify Power Enable 8 = HIGH	2	3.1093	3.5	Vdc
Pass	1388	K.4 Verify Power Enable 9 = HIGH	2	3.1138	3.5	Vdc
Pass	1389	K.4 Verify Power Enable 10 = HIGH	2	3.1149	3.5	Vdc
Pass	1390	K.4 Verify Power Enable 11 = HIGH	2	3.1137	3.5	Vdc
Pass	1391	K.4 Verify Power Enable 12 = HIGH	2	3.1226	3.5	Vdc
Pass	1392	K.4 Verify Power Enable 13 = HIGH	2	3.1215	3.5	Vdc
Pass	1396	N.1 Verify P12V5 Output	12.2	12.519	12.8	Vdc
Pass	1398	P.1 Verify P12V5 Short Circuit	-0.1	0.0010987	1	Vdc
Pass	1402	T.1 Verify P12V5 Output	12.2	12.519	12.8	Vdc
	1403	3.16.2 FAN Power Over-Current and short				
	1404	Set Initial Inputs to UUT for this test				
Pass	1423	Measure HB_BUS (V)	-0.5	0.008961	0.5	Vdc
Pass	1426	Measure P28V Bus	27.8	28	28.2	Vdc
	1427	Begin Test				
Pass	1437	D.1 Verify RR(3) FAN_CURR_LMT = LOW	0	0	0	Bool
Pass	1438	D.2 Verify FAN_PWR output	26.68	27.265	29.4	Vdc
Pass	1441	G.1 Verify FAN_PWR Short	-0.1	2.7099e-005	1	Vdc

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	1668	C. Verify PWR_EN_FBK_5 = HIGH	1	1	1	Bool
Pass	1669	C. Verify PWR_EN_FBK_6 = HIGH	1	1	1	Bool
Pass	1670	C. Verify PWR_EN_FBK_7 = HIGH	1	1	1	Bool
Pass	1671	C. Verify PWR_EN_FBK_8 = HIGH	1	1	1	Bool
Pass	1672	C. Verify PWR_EN_FBK_9 = HIGH	1	1	1	Bool
Pass	1673	C. Verify PWR_EN_FBK_10 = HIGH	1	1	1	Bool
Pass	1674	C. Verify PWR_EN_FBK_11 = HIGH	1	1	1	Bool
Pass	1675	C. Verify PWR_EN_FBK_12 = HIGH	1	1	1	Bool
Pass	1676	C. Verify PWR_EN_FBK_13 = HIGH	1	1	1	Bool
Pass	1677	D.1 Verify RR(10) PBIT_FLT_STS = LOW	0	0	0	Bool
Pass	1678	D.2 Verify RR(10) Main Only PBIT = HIGH	1	1	1	Bool
Pass	1683	F. Measure HB_BUS (V)	27.8	28.001	28.2	Vdc
Pass	1688	H.1 Verify RR(2) Master_State was = 0	0	0	0	Bool
Pass	1689	H.2 Verify RR(10) Main Only PBIT = LOW	0	0	0	Bool
	1692	3.18 Power Enable[0..13]				
	1693	Set Initial Inputs to UUT for this test				
Pass	1696	Measure P12V Backup_in (V)	11	11.993	13	Vdc
Pass	1714	Measure HB_BUS (V)	27	28.006	29	Vdc
Pass	1717	Measure P28V_BUS (V)	27	27.86	29	Vdc
	1718	Begin Test				
Pass	1725	A.1 Power Enable 0 = LOW	-0.1	0.022956	0.4	Vdc
Pass	1726	A.1 Power Enable 1 = LOW	-0.1	0.019315	0.4	Vdc
Pass	1727	A.1 Power Enable 2 = LOW	-0.1	0.020288	0.4	Vdc
Pass	1728	A.1 Power Enable 3 = LOW	-0.1	0.0185	0.4	Vdc
Pass	1729	A.1 Power Enable 4 = LOW	-0.1	0.023921	0.4	Vdc
Pass	1730	A.1 Power Enable 5 = LOW	-0.1	0.020916	0.4	Vdc
Pass	1731	A.1 Power Enable 6 = LOW	-0.1	0.023519	0.4	Vdc
Pass	1732	A.1 Power Enable 7 = LOW	-0.1	0.021695	0.4	Vdc
Pass	1733	A.1 Power Enable 8 = LOW	-0.1	0.023267	0.4	Vdc
Pass	1734	A.1 Power Enable 9 = LOW	-0.1	0.020815	0.4	Vdc
Pass	1735	A.1 Power Enable 10 = LOW	-0.1	0.024541	0.4	Vdc
Pass	1736	A.1 Power Enable 11 = LOW	-0.1	0.018918	0.4	Vdc
Pass	1737	A.1 Power Enable 12 = LOW	-0.1	0.023571	0.4	Vdc
Pass	1738	A.1 Power Enable 13 = LOW	-0.1	0.019924	0.4	Vdc
Pass	1739	A.2 Verify PW_EN_FBK_13 = HIGH	1	1	1	Bool
Pass	1740	A.3 Verify PW_EN_FBK_12 = HIGH	1	1	1	Bool
Pass	1741	A.4 Verify PW_EN_FBK_11 = HIGH	1	1	1	Bool
Pass	1742	A.5 Verify PW_EN_FBK_10 = HIGH	1	1	1	Bool
Pass	1743	A.6 Verify PW_EN_FBK_9 = HIGH	1	1	1	Bool
Pass	1744	A.7 Verify PW_EN_FBK_8 = HIGH	1	1	1	Bool
Pass	1745	A.8 Verify PW_EN_FBK_7 = HIGH	1	1	1	Bool
Pass	1746	A.9 Verify PW_EN_FBK_6 = HIGH	1	1	1	Bool
Pass	1747	A.10 Verify PW_EN_FBK_5 = HIGH	1	1	1	Bool
Pass	1748	A.11 Verify PW_EN_FBK_4 = HIGH	1	1	1	Bool
Pass	1749	A.12 Verify PW_EN_FBK_3 = HIGH	1	1	1	Bool
Pass	1750	A.13 Verify PW_EN_FBK_2 = HIGH	1	1	1	Bool
Pass	1751	A.14 Verify PW_EN_FBK_1 = HIGH	1	1	1	Bool
Pass	1752	A.15 Verify PW_EN_FBK_0 = HIGH	1	1	1	Bool
Pass	1755	C.1 Power Enable 0 = HIGH	2	3.0937	3.5	Vdc
Pass	1756	C.1 Power Enable 1 = HIGH	2	3.1008	3.5	Vdc
Pass	1757	C.1 Power Enable 2 = HIGH	2	3.1031	3.5	Vdc
Pass	1758	C.1 Power Enable 3 = HIGH	2	3.1017	3.5	Vdc

Status	Test	Test Description	Min.	Actual	Max.	Units
	1852	Set Initial Inputs to UUT for this test				
Pass	1855	Measure P12V Backup_in (V)	-1	-0.0016714	1	Vdc
Pass	1873	Measure HB_BUS (V)	-0.5	0.0096982	0.5	Vdc
Pass	1876	Measure P28V_BUS (V)	27	27.866	29	Vdc
	1877	Begin Test				
Pass	1886	B.1 Verify MODULE_PRESENT_14 = HIGH	1	1	1	Bool
Pass	1887	B.2 Verify MODULE_PRESENT_13 = HIGH	1	1	1	Bool
Pass	1888	B.3 Verify MODULE_PRESENT_12 = HIGH	1	1	1	Bool
Pass	1889	B.4 Verify MODULE_PRESENT_11 = HIGH	1	1	1	Bool
Pass	1890	B.5 Verify MODULE_PRESENT_10 = HIGH	1	1	1	Bool
Pass	1891	B.6 Verify MODULE_PRESENT_9 = HIGH	1	1	1	Bool
Pass	1892	B.7 Verify MODULE_PRESENT_8 = HIGH	1	1	1	Bool
Pass	1893	B.8 Verify MODULE_PRESENT_7 = HIGH	1	1	1	Bool
Pass	1894	B.9 Verify MODULE_PRESENT_6 = HIGH	1	1	1	Bool
Pass	1895	B.10 Verify MODULE_PRESENT_5 = HIGH	1	1	1	Bool
Pass	1896	B.11 Verify MODULE_PRESENT_4 = HIGH	1	1	1	Bool
Pass	1897	B.12 Verify MODULE_PRESENT_3 = HIGH	1	1	1	Bool
Pass	1898	B.13 Verify MODULE_PRESENT_2 = HIGH	1	1	1	Bool
Pass	1899	B.14 Verify MODULE_PRESENT_1 = HIGH	1	1	1	Bool
Pass	1900	B.15 Verify MODULE_PRESENT_0 = HIGH	1	1	1	Bool
Pass	1903	D.1 Verify MODULE_PRESENT_14 = LOW	0	0	0	Bool
Pass	1904	D.2 Verify MODULE_PRESENT_13 = LOW	0	0	0	Bool
Pass	1905	D.3 Verify MODULE_PRESENT_12 = LOW	0	0	0	Bool
Pass	1906	D.4 Verify MODULE_PRESENT_11 = LOW	0	0	0	Bool
Pass	1907	D.5 Verify MODULE_PRESENT_10 = LOW	0	0	0	Bool
Pass	1908	D.6 Verify MODULE_PRESENT_9 = LOW	0	0	0	Bool
Pass	1909	D.7 Verify MODULE_PRESENT_8 = LOW	0	0	0	Bool
Pass	1910	D.8 Verify MODULE_PRESENT_7 = LOW	0	0	0	Bool
Pass	1911	D.9 Verify MODULE_PRESENT_6 = LOW	0	0	0	Bool
Pass	1912	D.10 Verify MODULE_PRESENT_5 = LOW	0	0	0	Bool
Pass	1913	D.11 Verify MODULE_PRESENT_4 = LOW	0	0	0	Bool
Pass	1914	D.12 Verify MODULE_PRESENT_3 = LOW	0	0	0	Bool
Pass	1915	D.13 Verify MODULE_PRESENT_2 = LOW	0	0	0	Bool
Pass	1916	D.14 Verify MODULE_PRESENT_1 = LOW	0	0	0	Bool
Pass	1917	D.15 Verify MODULE_PRESENT_0 = LOW	0	0	0	Bool
	1918	3.21 HOT_SWAP				
	1919	Set Initial Inputs to UUT for this test				
Pass	1922	Measure P12V Backup_in (V)	-1	-0.0016374	1	Vdc
Pass	1940	Measure HB_BUS (V)	-0.5	0.0095861	0.5	Vdc
Pass	1943	Measure P28V_BUS (V)	27	27.866	29	Vdc
	1944	Begin Test				
Pass	1954	A. Measure HB_BUS (V)	27.8	28.002	28.2	Vdc
Pass	1955	A. Measure P12V Backup_in (V)	11	11.993	13	Vdc
Pass	1957	C.1 Verify RR(38) HOT_SWAP = LOW	0	0	0	Bool
Pass	1958	C.2 Verify RR(38) Crowbar = HIGH	1	1	1	Bool
Pass	1959	C.3 Verify P12V5 ~ 0V	-1	0.0023639	1	Vdc
Pass	1960	C.4 Power Enable 0 = HIGH	2	3.0967	3.5	Vdc
Pass	1961	C.4 Power Enable 1 = HIGH	2	3.1001	3.5	Vdc
Pass	1962	C.4 Power Enable 2 = HIGH	2	3.1022	3.5	Vdc
Pass	1963	C.4 Power Enable 3 = HIGH	2	3.0997	3.5	Vdc
Pass	1964	C.4 Power Enable 4 = HIGH	2	3.098	3.5	Vdc
Pass	1965	C.4 Power Enable 5 = HIGH	2	3.1	3.5	Vdc

Status	Test	Test Description	Min.	Actual	Max.	Units
	2142	N. Set P28V_BUS, HB_BUS = 19.8V				
Pass	2147	N. Measure P28V_BUS (V)	19.6	19.803	20	Vdc
Pass	2148	N. Measure HB_BUS (V)	19.6	19.809	20	Vdc
Pass	2150	P.1 Verify RR(10) PBIT_FLT_STS = LOW	0	0	0	Bool
Pass	2157	S.1 Verify P28V_BUS = 17.5V	17	17.759	18	Vdc
Pass	2158	S.2 P12V5 < 1V	-0.01	0.020744	1	Vdc
Pass	2164	U.1 P28V_BUS when 28MAIN_REDUN = HIGH	15.75	15.975	16.75	Vdc
Pass	2170	W. P28V_BUS when 28MAIN_REDUN = LOW	17.5	18.057	18.5	Vdc
Pass	2176	Y.1 P28V_BUS when P28V_LOCAL_LMT = HIGH	18.75	19.6	19.75	Vdc
Pass	2178	Y.2 Verify RR(10) PBIT_FLT_STS = LOW	0	0	0	Bool
Pass	2184	AA.1 HB_BUS when HB_LMT = LOW	17	17.404	18	Vdc
Pass	2190	AC.1 HB_BUS when HB_REDUN = HIGH	15.75	16.503	16.75	Vdc
Pass	2196	AE.1 HB_BUS when HB_REDUN = LOW	17.5	18.138	18.5	Vdc
Pass	2202	AG.1 HB_BUS when HB_LMT = HIGH	18.75	19.403	19.75	Vdc
Pass	2255	AJ.1 Verify RR(1) ON_OFF_BATT = HIGH	1	1	1	Bool
Pass	2256	AJ.2 Verify RR(10) FET_STATUS 3 = HIGH	1	1	1	Bool
Pass	2257	AJ.3 Verify RR(10) FET_STATUS 2 = HIGH	1	1	1	Bool
Pass	2258	AJ.4 Verify RR(10) FET_STATUS 1 = LOW	0	0	0	Bool
Pass	2259	AJ.5 Verify RR(10) FET_STATUS 0 = LOW	0	0	0	Bool
Pass	2260	AJ.6 Verify RR(2) BAT_PWR_TIMEOUT = LOW	0	0	0	Bool
Pass	2262	AK.1 Verify RR(2) BAT_PWR_TIMEOUT = HIGH	1	1	1	Bool
Pass	2263	AK.1 Verify RR(2) BAT_PWR_TIMEOUT = LOW	0	0	0	Bool
Pass	2265	AJ.7 HB T/O 11s	9	11	13	Sec
Pass	2269	AO.1 Verify RR(10) PBIT_FLT_STS = LOW	0	0	0	Bool
	2271	3.23 Battery Transfer Conditions				
	2272	Set Initial Inputs to UUT for this test				
Pass	2277	Measure P12V Backup_in (V)	11	11.932	13	Vdc
Pass	2295	Measure HB_BUS (V)	31	32.004	33	Vdc
Pass	2299	Measure P28V_BUS (V)	27	27.751	29	Vdc
	2300	Begin Test				
Pass	2308	A.1 Measure HB_BUS (V)	31.8	32.011	32.2	Vdc
Pass	2318	A.6 Measure P12V Backup_in (V)	11	11.998	13	Vdc
Pass	2319	A.6 Measure P28V_OFFSIDE (V)	2	3.2947	5	Vdc
	2320	B. Set P28V_BUS=28V				
Pass	2322	B. Verify P28V_BUS voltage	27.8	27.953	28.2	Vdc
Pass	2323	C.1 Verify RR(10) PBIT_FLT_STS = LOW	0	0	0	Bool
Pass	2324	C.2 Verify P12V5 output	12.2	12.494	12.8	Vdc
Pass	2325	C.3 Verify RR(10) FET_STATUS_0 = HIGH	1	1	1	Bool
Pass	2326	C.4 Verify RR(10) FET_STATUS_1 = HIGH	1	1	1	Bool
Pass	2327	C.5 Verify RR(10) FET_STATUS_2 = LOW	0	0	0	Bool
Pass	2328	C.6 Verify RR(10) FET_STATUS_3 = LOW	0	0	0	Bool
Pass	2329	C.7 Verify RR(39) CapableStateIn = 11	3	3	3	Bool
Pass	2396	F.1 P12V5 Trans Max	12	12.64	13	Vdc
Pass	2397	F.1 P12V5 Trans Min	12	12.48	13	Vdc
Pass	2398	F.1 Verify running on HB_BUS	10	24.612	60	Adc
	2405	G. Reapply P28V_BUS				
Pass	2408	G.1 P12V5 Trans Max	12	12.56	13	Vdc
Pass	2409	G.1 P12V5 Trans Min	12	12.4	13	Vdc
Pass	2410	G.2 Verify P12V5 output	12.2	12.494	12.8	Vdc
Pass	2423	M.1 operation on HB_BUS	10.81	10.951	11	Sec
Pass	2425	M.2 HB_BUS Shutdown	2	21.1	30	ms
Pass	2427	M.3 Verify P28V MAIN MONITOR FAULT = LOW	0	0	0	Bool

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	2604	G.3 Power Enable 12 = LOW	-0.1	0.022752	0.4	Vdc
Pass	2605	G.3 Power Enable 13 = LOW	-0.1	0.01912	0.4	Vdc
Pass	2607	G.4 Verify FAN_INHIBIT_PIN = HIGH	1	1	1	Bool
Pass	2608	G.5 Verify FAN power output	26.68	28.082	29.4	Vdc
Pass	2617	G.6 Verify start of reset period	0.3	0.32544	0.8	Sec
Pass	2637	H.1 Verify P12V_Backup out is on: setting #2	11.5	11.942	12.5	Vdc
Pass	2637	H.2 Verify P12V_Backup out is on: setting #3	11.5	11.942	12.5	Vdc
Pass	2637	H.3 Verify P12V_Backup out is on: setting #4	11.5	11.942	12.5	Vdc
Pass	2637	H.4 Verify P12V_Backup out is on: setting #5	11.5	11.942	12.5	Vdc
Pass	2637	H.5 Verify P12V_Backup out is on: setting #6	11.5	11.942	12.5	Vdc
Pass	2637	H.6 Verify P12V_Backup out is on: setting #7	11.5	11.943	12.5	Vdc
Pass	2641	I.1 Verify P12V_Backup out is on: setting #8	11.5	11.943	12.5	Vdc
Pass	2651	J.1 Verify P12V_Backup out is off: setting #9	-1	0.0075357	1	Vdc
Pass	2654	J.1 Verify P12V_Backup recovers from reset	11.5	11.942	12.5	Vdc
Pass	2651	J.2 Verify P12V_Backup out is off: setting #10	-1	0.0069033	1	Vdc
Pass	2654	J.2 Verify P12V_Backup recovers from reset	11.5	11.942	12.5	Vdc
Pass	2657	K.1 Verify P12V_Backup out off setting: 11	-1	0.0085049	1	Vdc
Pass	2659	K.1 Verify P12V_Backup out remains off (5s)	-1	0.00094056	1	Vdc
Pass	2661	K.1 Verify P12V_Backup out remains off (10s)	-1	0.0004489	1	Vdc
Pass	2664	M Verify P12V_5 recovers after reset	12.2	12.509	12.8	Vdc
	2665	3.25 MOD_DISC[10..13]				
	2666	Set Initial Inputs to UUT for this test				
Pass	2670	Measure P28V_BUS (V)	27.8	27.947	28.2	Vdc
	2671	Begin Test				
Pass	2682	C.1 A read was succesful?	1	1	1	Bool
	2684	3.26 Real Time Clock				
	2685	Set Initial Inputs to UUT for this test				
Pass	2688	Measure P12V Backup_in (V)	11	11.995	13	Vdc
Pass	2706	Measure HB_BUS (V)	35.8	36.018	36.2	Vdc
Pass	2709	Measure P28V_BUS (V)	27.8	27.948	28.2	Vdc
	2710	Begin Test				
	2719	B. Set Output loads to no load				
Pass	2731	H.1 Verify RTC is at current time	-1	0	1	Sec
Pass	2736	K. Verify Battery RTC Battery current draw	8	13.43	25	mA
	2737	3.27 Bit and Partial Power				
	2738	Set Initial Inputs to UUT for this test				
Pass	2741	Measure P12V Backup_in (V)	11	11.933	13	Vdc
Pass	2759	Measure HB_BUS (V)	-1	0.013312	1	Vdc
Pass	2762	Measure P28V_BUS (V)	-1	0.046246	1	Vdc
	2763	Begin Test				
	2790	E. P12V_BCK_IN_V BIT "+" going				
Pass	2791	E.1 Verify RR(1) P12V_BACK_LMT = LOW	0	0	0	Bool
Pass	2792	E.3 Verify in GPM mode	3	3	3	Bool
Pass	2800	E.1 Verify RR(1) P12V_BACK_LMT = HIGH	1	1	1	Bool
Pass	2801	E.1 Verify P12V_BCK_IN	10	11.223	11.4	Vdc
Pass	2802	E.3 Verify in GPM mode	3	3	3	Bool
Pass	2809	E.2 Verify RR(1) P12V_BACK_LMT = LOW	0	0	0	Bool
Pass	2810	E.2 Verify P12V_BCK_IN	12.6	13.021	13.1	Vdc
Pass	2811	E.3 Verify in GPM mode	3	3	3	Bool
Pass	2818	E.3 Verify in GPM mode	3	3	3	Bool
Pass	2819	E.4 Verify P12V_BCK_IN	14	14.107	14.2	Vdc
Pass	2821	E.4 Verify P12V_BCK_IN current	2	77.31	90	mVolts

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	3036	D.1 Verify Width when high	0.000475	0.00050004	0.000525	Secs
Pass	3038	D.2 Verify Width when Low	0.000475	0.00050004	0.000525	Secs
Pass	3039	D.3 Verify maximum voltage	3	3.305	6	Volts
Pass	3040	D.4 Verify Minimum voltage	-0.1	0	0.6	Volts
	3042	3.29 Power on Timing				
	3043	Set Initial Inputs to UUT for this test				
Pass	3046	Measure P12V Backup_in (V)	11	11.995	13	Vdc
Pass	3064	Measure HB_BUS (V)	27.8	27.985	28.2	Vdc
Pass	3067	Measure P28V_BUS (V)	-1	0.047225	1	Vdc
	3068	Begin Test				
Pass	3084	3.29.C.1 Verify P12V5 regulates in < 1s	-1	0.4748	1	Sec
Pass	3099	3.29.E.1 Verify P12VBK out is up before P12V5	0.005	0.020064	1	Sec
	3101	3.30 Load Transient on P12V5				
	3102	Set Initial Inputs to UUT for this test				
Pass	3105	Measure P12V Backup_in (V)	11	11.998	13	Vdc
Pass	3123	Measure HB_BUS (V)	27	28.011	29	Vdc
Pass	3126	Measure P28V_BUS (V)	27	27.894	29	Vdc
	3127	Begin Test				
Pass	3142	C.1 Maximum	-0.3	0.056	0.3	Vac
Pass	3143	C.1 & C.2 Minimum	-0.3	-0.097	0.3	Vac
Pass	3151	E.1 Maximum	-0.3	0.066	0.3	Vac
Pass	3152	E.1 Minimum	-0.3	-0.097	0.3	Vac

Status	Test	Test Description	Min.	Actual	Max.	Units
	2822	F. P12V_BCK_IN_V BIT "-" going				
Pass	2830	F.1 Verify RR(1) P12V_BACK_LMT = HIGH	1	1	1	Bool
Pass	2831	F.1 Verify P12V_BCK_IN	12.6	12.723	13.1	Vdc
Pass	2832	F.3 Verify in GPM mode	3	3	3	Bool
Pass	2839	F.2 Verify RR(1) P12V_BACK_LMT = LOW	0	0	0	Bool
Pass	2840	F.2 Verify P12V_BCK_IN	10	10.823	11.4	Vdc
Pass	2841	F.3 Verify in GPM mode	3	3	3	Bool
Pass	2843	H Verify FAN power OFF	-1	0.0012675	1	Vdc
Pass	2847	H Verify FAN Power	18	20.488	22	Vdc
	2848	I. FAN_V BIT "+" going				
Pass	2849	I.1 Verify RR(3) FAN_VOLTAGE_LMT = LOW	0	0	0	Bool
Pass	2857	I.1 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	2858	I.1 Verify FAN Power	25.5	26.43	26.67	Vdc
Pass	2865	I.2 Verify RR(3) FAN_VOLTAGE_LMT = LOW	0	0	0	Bool
Pass	2866	I.2 Verify FAN Power	29.4	30.224	30.7	Vdc
	2867	J. FAN_V BIT "-" going				
Pass	2874	J.1 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	2875	J.1 Verify FAN Power	29.4	29.916	30.7	Vdc
Pass	2882	J.2 Verify RR(3) FAN_VOLTAGE_LMT = LOW	0	0	0	Bool
Pass	2883	J.2 Verify FAN Power	25.5	25.709	26.67	Vdc
	2889	L. CV_V BIT "+" going				
Pass	2890	L.1 Verify RR(4) CV_Voltage_LMT = LOW	0	0	0	Bool
Pass	2898	L.1 Verify RR(4) CV_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	2899	L.1 Verify CV Power	25.5	26.147	26.75	Vdc
Pass	2906	L.2 Verify RR(4) CV_VOLTAGE_LMT = LOW	0	0	0	Bool
Pass	2907	L.2 Verify CV Power	29.3	30.049	30.8	Vdc
	2908	M. CV_V BIT "-" going				
Pass	2915	M.1 Verify RR(4) CV_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	2916	M.1 Verify CV Power	29.3	29.843	30.8	Vdc
Pass	2923	M.2 Verify RR(4) CV_VOLTAGE_LMT = LOW	0	0	0	Bool
Pass	2924	M.2 Verify CV Power	25.5	25.942	26.75	Vdc
Pass	2930	N. Verify UUT still in AUTO mode.	2	2	2	Bool
Pass	2935	S.1 Verify P12V5 Power is Off	-1	0.016376	1	Vdc
	2939	U. P12V5_V BIT "+" going				
Pass	2940	U.1 Verify RR(1) P12V5_LMT = LOW	0	0	0	Bool
Pass	2948	U.1 Verify RR(1) P12V5_LMT = HIGH	1	1	1	Bool
Pass	2949	U.1 Verify P12V5 Power	10	10.577	12.19	Vdc
Pass	2956	U.2 Verify RR(1) P12V5_LMT = LOW	0	0	0	Bool
Pass	2957	U.2 Verify P12V5 Power	12.81	13.578	14	Vdc
	2958	V. P12V5_V BIT "-" going				
Pass	2965	V.1 Verify RR(1) P12V5_LMT = HIGH	1	1	1	Bool
Pass	2966	V.1 Verify P12V5 Power	12.81	13.181	14	Vdc
Pass	2973	V.2 Verify RR(1) P12V5_LMT = LOW	0	0	0	Bool
Pass	2974	V.2 Verify P12V5 Power	10	10.175	12.19	Vdc
Pass	2982	X. Verify RR(4) CV_LMT_SHUTDN = LOW & flickers	1	1	1	Bool
Pass	2985	Z.1 Read RR(4) CV_LMT_SHUTDN	1	1	1	Bool
	2995	3.28 P28V_Main_OK_OUT_Timing				
	2996	Set Initial Inputs to UUT for this test				
Pass	2999	Measure P12V Backup_in (V)	11.8	11.995	12.2	Vdc
Pass	3017	Measure HB_BUS (V)	35.8	36.013	36.2	Vdc
Pass	3020	Measure P28V_BUS (V)	27.5	27.951	28.5	Vdc
	3021	Begin Test				

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	2428	M.4 Verify Battery Leakage Current	0.1	0.27561	7	mA
Pass	2433	N. Measure HB_BUS (V)	-1	0.012445	1	Vdc
Pass	2434	N. Measure P12V Backup_in (V)	-1	-0.00136	1	Vdc
Pass	2439	O. Measure HB_BUS (V)	31.5	32.01	32.5	Vdc
Pass	2440	P.1 Verify RR(10) PBIT_FLT_STS = LOW	0	0	0	Bool
Pass	2441	P.2 Verify Battery Leakage Current	0.1	0.51418	7	mA
Pass	2448	R. Measure P28V_OFFSIDE_LMT (V)	-1	0.7221	1	Vdc
Pass	2449	S.1 Verify RR(39) CapableStateIn = 00	0	0	0	Bool
Pass	2458	V.1 Verify running on HB_BUS	10	14.955	60	Adc
Pass	2463	Verify P28V_OFFSIDE_LMT is High	2	3.298	5.5	Vdc
Pass	2464	X.1 Verify running on HB_BUS	10	14.953	60	Adc
Pass	2469	AA.1 Verify running on HB_BUS	1	14.842	60	Adc
Pass	2472	AC.1 Verify not running on HB_BUS	-1	0	0.5	Adc
Pass	2478	AE.1 Verify RR(39) CapableStateIN = 10	2	2	2	Bool
	2483	3.24 Reset Operation				
	2484	Set Initial Inputs to UUT for this test				
Pass	2503	Measure HB_BUS (V)	31	32.014	33	Vdc
Pass	2506	Measure P28V_BUS (V)	-1	0.042993	1	Vdc
	2507	Begin Test				
	2515	B. Set Output loads to no load				
Pass	2520	C.1 Verify P12V5 output	12.2	12.489	12.8	Vdc
Pass	2530	F.1 Verify P12V5 low	-1	-0.19	1	Volts
Pass	2542	F.2 Power Enable 0 = HIGH	2	3.06	3.5	Volts
Pass	2542	F.2 Power Enable 1 = HIGH	2	3.06	3.5	Volts
Pass	2542	F.2 Power Enable 2 = HIGH	2	3.06	3.5	Volts
Pass	2542	F.2 Power Enable 3 = HIGH	2	3.06	3.5	Volts
Pass	2542	F.2 Power Enable 4 = HIGH	2	3.06	3.5	Volts
Pass	2542	F.2 Power Enable 5 = HIGH	2	3.06	3.5	Volts
Pass	2553	F.2 Power Enable 6 = HIGH	2	3.06	3.5	Volts
Pass	2553	F.2 Power Enable 7 = HIGH	2	3.06	3.5	Volts
Pass	2553	F.2 Power Enable 8 = HIGH	2	3.06	3.5	Volts
Pass	2553	F.2 Power Enable 9 = HIGH	2	3.06	3.5	Volts
Pass	2553	F.2 Power Enable 10 = HIGH	2	3.06	3.5	Volts
Pass	2553	F.2 Power Enable 11 = HIGH	2	3.06	3.5	Volts
Pass	2564	F.2 Power Enable 12 = HIGH	2	3.06	3.5	Volts
Pass	2564	F.2 Power Enable 13 = HIGH	2	3.06	3.5	Volts
Pass	2574	F.3 CV_INHIBIT_OUT low	-0.1	0	0.5	Volts
Pass	2586	F.4 Verify that FPGA read did not work	-9999	-9999	-9999	Decimal
Pass	2589	G.1 Verify reset period	1	2.6732	5	Sec
Pass	2591	G.2 Verify P12V5 output	12.2	12.509	12.8	Vdc
Pass	2592	G.3 Power Enable 0 = LOW	-0.1	0.022218	0.4	Vdc
Pass	2593	G.3 Power Enable 1 = LOW	-0.1	0.018595	0.4	Vdc
Pass	2594	G.3 Power Enable 2 = LOW	-0.1	0.019572	0.4	Vdc
Pass	2595	G.3 Power Enable 3 = LOW	-0.1	0.017783	0.4	Vdc
Pass	2596	G.3 Power Enable 4 = LOW	-0.1	0.023174	0.4	Vdc
Pass	2597	G.3 Power Enable 5 = LOW	-0.1	0.020163	0.4	Vdc
Pass	2598	G.3 Power Enable 6 = LOW	-0.1	0.022757	0.4	Vdc
Pass	2599	G.3 Power Enable 7 = LOW	-0.1	0.02094	0.4	Vdc
Pass	2600	G.3 Power Enable 8 = LOW	-0.1	0.022506	0.4	Vdc
Pass	2601	G.3 Power Enable 9 = LOW	-0.1	0.020029	0.4	Vdc
Pass	2602	G.3 Power Enable 10 = LOW	-0.1	0.023752	0.4	Vdc
Pass	2603	G.3 Power Enable 11 = LOW	-0.1	0.018134	0.4	Vdc

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	1966	C.4 Power Enable 6 = HIGH	2	3.0909	3.5	Vdc
Pass	1967	C.4 Power Enable 7 = HIGH	2	3.0973	3.5	Vdc
Pass	1968	C.4 Power Enable 8 = HIGH	2	3.0859	3.5	Vdc
Pass	1969	C.4 Power Enable 9 = HIGH	2	3.0907	3.5	Vdc
Pass	1970	C.4 Power Enable 10 = HIGH	2	3.0911	3.5	Vdc
Pass	1971	C.4 Power Enable 11 = HIGH	2	3.0905	3.5	Vdc
Pass	1972	C.4 Power Enable 12 = HIGH	2	3.0981	3.5	Vdc
Pass	1973	C.4 Power Enable 13 = HIGH	2	3.0967	3.5	Vdc
Pass	1974	C.5 Verify RR(10) FET_STATUS 0 = LOW	0	0	0	Bool
Pass	1975	C.6 Verify RR(10) FET_STATUS 1 = LOW	0	0	0	Bool
Pass	1976	C.7 Verify RR(10) FET_STATUS 2 = LOW	0	0	0	Bool
Pass	1977	C.8 Verify RR(10) FET_STATUS 3 = LOW	0	0	0	Bool
Pass	1981	G.1 Verify P12V5 = 12.5 +/- 0.3V	12.2	12.519	12.8	Vdc
	1983	3.22 Hot Battery, P12V_BACKUP_IN and Pwr Transfer				
Pass	1989	Measure P12V Backup_in (V)	-1	-0.0015121	1	Vdc
Pass	2007	Measure HB_BUS (V)	27	28.007	29	Vdc
Pass	2011	Measure P28V_BUS (V)	27	27.858	29	Vdc
	2012	Begin Test				
Pass	2023	A. Measure HB_BUS (V)	27.8	28.009	28.2	Vdc
Pass	2024	A. Measure P28V_BUS (V)	27.8	28.062	28.2	Vdc
	2025	B. Set Output loads to full load				
Pass	2035	C.1 Measure P12V Backup_in (V)	11	11.997	13	Vdc
Pass	2036	C.2 Measure P28V_OFFSIDE_LMT (V)	-1	0.72241	1	Vdc
Pass	2037	F.1 Verify PBIT_FLT_STS = LOW	0	0	0	Bool
Pass	2041	G. Verify GPM Mode	3	3	3	Bool
Pass	2042	H.1 Verify P12V5 output	12.2	12.502	12.8	Vdc
Pass	2043	H.2 Verify P12V_BACKUP_OUT	11.52	11.911	12.48	Vdc
Pass	2044	H.3 Verify FET_STATUS_0 = HIGH	1	1	1	Bool
Pass	2045	H.4 Verify FET_STATUS_1 = HIGH	1	1	1	Bool
Pass	2046	H.5 Verify FET_STATUS_2 = LOW	0	0	0	Bool
Pass	2047	H.6 Verify FET_STATUS_3 = LOW	0	0	0	Bool
Pass	2048	H.7 Verify P12V_BACK_LMT = HIGH	1	1	1	Bool
Pass	2051	H.8 Verify P12V_BCK_IN current	0	0.0002821	0.002	Adc
Pass	2116	J.1 Verify P12V5 output	12.2	12.501	12.8	Vdc
Pass	2118	J.1 P12V5 Trans Max	12	12.64	13	Vdc
Pass	2119	J.1 P12V5 Trans Min	12	12.48	13	Vdc
Pass	2120	J.2 HB_BUS Current (PCM Running on HB_BUS)	25	35.547	60	Adc
Pass	2121	J.3 Verify RR(10) FET_STATUS_3 = HIGH	1	1	1	Bool
Pass	2122	J.4 Verify RR(10) FET_STATUS_2 = HIGH	1	1	1	Bool
Pass	2123	J.5 Verify RR(10) FET_STATUS_1 = LOW	0	0	0	Bool
Pass	2124	J.6 Verify RR(10) FET_STATUS_0 = LOW	0	0	0	Bool
Pass	2125	J.7 RR(1) ON_OFF_BATTERY = HIGH	1	1	1	Bool
Pass	2127	K.1 Verify P12V5 < 1V	-0.1	0.0093777	1	Vdc
Pass	2128	K.2 (RBW0) SWTR_ENABLE = LOW	0	0	0	Bool
Pass	2129	K.3 Verify FET_STATUS_3 = LOW	0	0	0	Bool
Pass	2130	K.4 Verify FET_STATUS_2 = LOW	0	0	0	Bool
Pass	2131	K.5 Verify FET_STATUS_1 = LOW	0	0	0	Bool
Pass	2132	K.6 Verify FET_STATUS_0 = LOW	0	0	0	Bool
Pass	2133	K.7 Verify RR(2) MASTER_STATE = 11 (GPM)	3	3	3	Bool
Pass	2136	L. Measure P12V Backup_in (V)	-1	-0.0013794	1	Vdc
Pass	2139	L. Measure P12V Backup_in (V)	11	11.931	13	Vdc
Pass	2140	M.1 Verify RR(2) MASTER_STATE = 00 (PBIT)	0	0	0	Bool

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	1759	C.1 Power Enable 4 = HIGH	2	3.0995	3.5	Vdc
Pass	1760	C.1 Power Enable 5 = HIGH	2	3.1024	3.5	Vdc
Pass	1761	C.1 Power Enable 6 = HIGH	2	3.0929	3.5	Vdc
Pass	1762	C.1 Power Enable 7 = HIGH	2	3.0998	3.5	Vdc
Pass	1763	C.1 Power Enable 8 = HIGH	2	3.0884	3.5	Vdc
Pass	1764	C.1 Power Enable 9 = HIGH	2	3.0929	3.5	Vdc
Pass	1765	C.1 Power Enable 10 = HIGH	2	3.093	3.5	Vdc
Pass	1766	C.1 Power Enable 11 = HIGH	2	3.0924	3.5	Vdc
Pass	1767	C.1 Power Enable 12 = HIGH	2	3.1	3.5	Vdc
Pass	1768	C.1 Power Enable 13 = HIGH	2	3.0989	3.5	Vdc
Pass	1769	C.2 Verify PW_EN_FBK_13 = LOW	0	0	0	Bool
Pass	1770	C.3 Verify PW_EN_FBK_12 = LOW	0	0	0	Bool
Pass	1771	C.4 Verify PW_EN_FBK_11 = LOW	0	0	0	Bool
Pass	1772	C.5 Verify PW_EN_FBK_10 = LOW	0	0	0	Bool
Pass	1773	C.6 Verify PW_EN_FBK_9 = LOW	0	0	0	Bool
Pass	1774	C.7 Verify PW_EN_FBK_8 = LOW	0	0	0	Bool
Pass	1775	C.8 Verify PW_EN_FBK_7 = LOW	0	0	0	Bool
Pass	1776	C.9 Verify PW_EN_FBK_6 = LOW	0	0	0	Bool
Pass	1777	C.10 Verify PW_EN_FBK_5 = LOW	0	0	0	Bool
Pass	1778	C.11 Verify PW_EN_FBK_4 = LOW	0	0	0	Bool
Pass	1779	C.12 Verify PW_EN_FBK_3 = LOW	0	0	0	Bool
Pass	1780	C.13 Verify PW_EN_FBK_2 = LOW	0	0	0	Bool
Pass	1781	C.14 Verify PW_EN_FBK_1 = LOW	0	0	0	Bool
Pass	1782	C.15 Verify PW_EN_FBK_0 = LOW	0	0	0	Bool
	1783	3.19 SWTR_ENABLE				
	1784	Set Initial Inputs to UUT for this test				
Pass	1787	Measure P12V Backup_in (V)	11	11.993	13	Vdc
Pass	1805	Measure HB_BUS (V)	27	28.009	29	Vdc
Pass	1808	Measure P28V_BUS (V)	27	27.859	29	Vdc
	1809	Begin Test				
Pass	1816	A. Verify P12V5 is On	12.2	12.518	12.8	Vdc
Pass	1819	B.1 Verify P12V5 Shuts down	-1	0.28246	1	Vdc
Pass	1820	B.2 Verify RBW(0) SWTR_EN = Low	0	0	0	Bool
Pass	1822	D.1 Verify P12V5 is On	12.2	12.513	12.8	Vdc
Pass	1826	E. Measure HB_BUS (V)	-0.5	0.011018	0.5	Vdc
Pass	1827	F. Measure P12V Backup_in (V)	-1	-0.0016188	1	Vdc
	1830	H. Toggle P28V BUS				
Pass	1835	I.1 Power Enable 0 = LOW	-0.1	0.023003	0.4	Vdc
Pass	1836	I.1 Power Enable 1 = LOW	-0.1	0.019357	0.4	Vdc
Pass	1837	I.1 Power Enable 2 = LOW	-0.1	0.02033	0.4	Vdc
Pass	1838	I.1 Power Enable 3 = LOW	-0.1	0.01854	0.4	Vdc
Pass	1839	I.1 Power Enable 4 = LOW	-0.1	0.02397	0.4	Vdc
Pass	1840	I.1 Power Enable 5 = LOW	-0.1	0.020959	0.4	Vdc
Pass	1841	I.1 Power Enable 6 = LOW	-0.1	0.023564	0.4	Vdc
Pass	1842	I.1 Power Enable 7 = LOW	-0.1	0.021707	0.4	Vdc
Pass	1843	I.1 Power Enable 8 = LOW	-0.1	0.023315	0.4	Vdc
Pass	1844	I.1 Power Enable 9 = LOW	-0.1	0.020859	0.4	Vdc
Pass	1845	I.1 Power Enable 10 = LOW	-0.1	0.024585	0.4	Vdc
Pass	1846	I.1 Power Enable 11 = LOW	-0.1	0.01896	0.4	Vdc
Pass	1847	I.1 Power Enable 12 = LOW	-0.1	0.023606	0.4	Vdc
Pass	1848	I.1 Power Enable 13 = LOW	-0.1	0.019957	0.4	Vdc
	1851	3.20 MODULE_PRESENT[0..14]				

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	1444	J. Verify FAN_PWR output	26.68	27.652	29.4	Vdc
	1445	3.16.3 CV Power Over-Current and Short				
	1446	Set Initial Inputs to UUT for this test				
Pass	1465	Measure HB_BUS (V)	-0.5	0.0093697	0.5	Vdc
Pass	1468	Measure P28V Bus	27.8	28	28.2	Vdc
	1469	Begin Test				
Pass	1525	C. PCM in Auto mode?	2	2	2	Bool
Pass	1533	D.1. CV_PWR on 60ms	0.058	0.059594	0.062	Sec
Pass	1546	D.2 Verify CV_CURR_LMT Toggling	1	1	1	Bool
Pass	1547	D.3 Verify CV_LMT_SHUTDN Low mostly	1	1	1	Bool
Pass	1550	E.1 CV_LMT_SHUTDN = HIGH	1	1	1	Bool
Pass	1554	G.1 Verify CV_PWR output	-29.12	-27.919	-26.8	Vdc
Pass	1556	I.1 Verify CV_PWR Short	-1	-2.3297e-005	1	Vdc
Pass	1559	K.1 Verify CV_PWR output	-29.12	-27.919	-26.8	Vdc
Pass	1564	M Verify CV_PWR output	26.8	27.922	29.12	Vdc
Pass	1566	N.1 Verify CV_PWR Short	-1	-1.158e-005	1	Vdc
Pass	1570	P.1 Verify CV_PWR output	26.8	27.922	29.12	Vdc
	1571	3.16.4 12VBCK Over-Current and Short				
	1572	Set Initial Inputs to UUT for this test				
Pass	1591	Measure HB_BUS (V)	-0.5	0.0092695	0.5	Vdc
Pass	1594	Measure P28V_BUS (V)	27	27.851	29	Vdc
	1595	Begin Test				
Pass	1599	B.1 Verify P12V5 output	12.2	12.51	12.8	Vdc
Pass	1600	B.2 Verify P12V_BACKUP_OUT = 0V	-1	0.0081935	1	Vdc
Pass	1603	D. Verify P12V_BACKUP_OUT output	11.52	11.916	12.48	Vdc
Pass	1605	F. Verify P12V_BACKUP_OUT is shorted	-1	-8.9524e-005	1	Vdc
Pass	1608	H. Verify P12V_BACKUP_OUT output	11.52	11.916	12.48	Vdc
	1609	3.17 Triggered PBIT				
	1610	Set Initial Inputs to UUT for this test				
Pass	1629	Measure HB_BUS (V)	-0.5	0.0094544	0.5	Vdc
Pass	1632	Measure P28V_BUS (V)	27	27.855	29	Vdc
	1633	Begin Test				
Pass	1641	A. Measure P12V Backup_in (V)	11	11.993	13	Vdc
Pass	1648	C. Verify PWR_EN_FBK_0 = Low	0	0	0	Bool
Pass	1649	C. Verify PWR_EN_FBK_1 = Low	0	0	0	Bool
Pass	1650	C. Verify PWR_EN_FBK_2 = Low	0	0	0	Bool
Pass	1651	C. Verify PWR_EN_FBK_3 = Low	0	0	0	Bool
Pass	1652	C. Verify PWR_EN_FBK_4 = Low	0	0	0	Bool
Pass	1653	C. Verify PWR_EN_FBK_5 = Low	0	0	0	Bool
Pass	1654	C. Verify PWR_EN_FBK_6 = Low	0	0	0	Bool
Pass	1655	C. Verify PWR_EN_FBK_7 = Low	0	0	0	Bool
Pass	1656	C. Verify PWR_EN_FBK_8 = Low	0	0	0	Bool
Pass	1657	C. Verify PWR_EN_FBK_9 = Low	0	0	0	Bool
Pass	1658	C. Verify PWR_EN_FBK_10 = Low	0	0	0	Bool
Pass	1659	C. Verify PWR_EN_FBK_11 = Low	0	0	0	Bool
Pass	1660	C. Verify PWR_EN_FBK_12 = Low	0	0	0	Bool
Pass	1661	C. Verify PWR_EN_FBK_13 = Low	0	0	0	Bool
Pass	1663	C. Verify PWR_EN_FBK_0 = HIGH	1	1	1	Bool
Pass	1664	C. Verify PWR_EN_FBK_1 = HIGH	1	1	1	Bool
Pass	1665	C. Verify PWR_EN_FBK_2 = HIGH	1	1	1	Bool
Pass	1666	C. Verify PWR_EN_FBK_3 = HIGH	1	1	1	Bool
Pass	1667	C. Verify PWR_EN_FBK_4 = HIGH	1	1	1	Bool

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	1079	I.1 Verify CV_PWR Holding current 10 to 20 mA	10	11.837	20	mA
Pass	1081	K.1 Verify CV_PWR is off	-1	9.878e-006	1	Vdc
	1082	3.13 Control Valve Error				
	1083	Set Initial Inputs to UUT for this test				
Pass	1102	Measure HB_BUS (V)	-0.5	0.0084791	0.5	Vdc
Pass	1104	Verify P28V_BUS Voltage	27.8	27.997	28.2	Vdc
	1105	Begin Test				
Pass	1117	D.1 Verify CV_PWR Voltage	26.8	27.928	29.12	Vdc
Pass	1122	H.1 Verify CV_PWR NOT on	-1	1.0102e-005	1	Vdc
Pass	1123	H.2 Verify (RBW4) CV_ON_PIN = LOW	0	0	0	Bool
Pass	1125	J.1 Verify RR(4) CV_POS = 00 (ERROR)	0	0	0	Bool
	1127	3.14 CV_INHIBIT_OUT				
	1128	Set Initial Inputs to UUT for this test				
Pass	1147	Measure HB_BUS (V)	-0.5	0.0084568	0.5	Vdc
Pass	1150	Set P28V_BUS Voltage	27.8	27.998	28.2	V
	1151	Begin Test				
Pass	1164	B.1 Verify CV_INHIBIT_OUT Toggling	1	1	1	Bool
Pass	1165	C.1 Verify CV_INHIBIT_PIN Toggling	1	1	1	Bool
Pass	1169	G.1 IO Verify CV_INHIBIT_OUT = off	-0.5	-0.0024903	0.5	Vdc
Pass	1170	H.1 Verify (RBW4) CV_INHIBIT = LOW	0	0	0	Bool
Pass	1172	J.1 IO Verify CV_INHIBIT_OUT = ON	3.1	3.298	3.5	Vdc
Pass	1173	K.1 Verify (RBW4) CV_INHIBIT_PIN = HIGH	1	1	1	Bool
	1177	3.15 In-Rush Current				
	1178	Set Initial Inputs to UUT for this test				
Pass	1197	Measure HB_BUS (V)	-0.5	0.0082372	0.5	Vdc
	1198	Begin Test				
Pass	1204	A. Measure P28V Bus	19.9	19.979	20.1	Vdc
Pass	1259	E.1 Verify Inrush < 100A in first 100ms	20	39.2	100	Adc
Pass	1271	E.2 Verify Inrush < 80A after first 100ms	20	49.6	80	Adc
	1272	3.16 Power Output Over-Current and Short Tests				
	1273	3.16.1 12.5 Power Output Over-Current and Short				
	1274	Set Initial Inputs to UUT for this test				
Pass	1293	Measure HB_BUS (V)	-0.5	0.0055789	0.5	Vdc
Pass	1296	Verify P28V_BUS	27.8	27.964	28.2	Vdc
	1297	Begin Test				
Pass	1313	F.1 Verify RR(39) P12V5_OC = LOW	0	0	0	Bool
Pass	1314	F.2 Verify (RBW0) SWTR_ENABLE = HIGH	1	1	1	Bool
Pass	1315	F.3 Verify P12V5 Output Voltage	12.2	12.516	12.8	Vdc
Pass	1317	G. Verify Power Enable 0 = LOW	-0.1	0.022772	0.4	Vdc
Pass	1318	G. Verify Power Enable 1 = LOW	-0.1	0.019122	0.4	Vdc
Pass	1319	G. Verify Power Enable 2 = LOW	-0.1	0.020101	0.4	Vdc
Pass	1320	G. Verify Power Enable 3 = LOW	-0.1	0.018307	0.4	Vdc
Pass	1321	G. Verify Power Enable 4 = LOW	-0.1	0.023758	0.4	Vdc
Pass	1322	G. Verify Power Enable 5 = LOW	-0.1	0.020732	0.4	Vdc
Pass	1323	G. Verify Power Enable 6 = LOW	-0.1	0.023346	0.4	Vdc
Pass	1324	G. Verify Power Enable 7 = LOW	-0.1	0.021524	0.4	Vdc
Pass	1325	G. Verify Power Enable 8 = LOW	-0.1	0.023096	0.4	Vdc
Pass	1326	G. Verify Power Enable 9 = LOW	-0.1	0.020656	0.4	Vdc
Pass	1327	G. Verify Power Enable 10 = LOW	-0.1	0.024386	0.4	Vdc
Pass	1328	G. Verify Power Enable 11 = LOW	-0.1	0.018762	0.4	Vdc
Pass	1329	G. Verify Power Enable 12 = LOW	-0.1	0.023422	0.4	Vdc
Pass	1330	G. Verify Power Enable 13 = LOW	-0.1	0.019756	0.4	Vdc

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Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	720	F.4 Verify P12V_BACKUP_OUT Voltage	11.52	11.911	12.48	Vdc
Pass	722	F.5 Verify P12V_BACKUP_OUT Ripple	10	30.49	100	mVolts
Pass	724	F.6 PCM Efficiency	80	85.058	95	%
	725	Set P28V_BUS				
Pass	727	G. Measure P28V_BUS	35.8	35.984	36.2	Vdc
Pass	731	I.1 Verify P12V5 Pk-Pk Ripple	10	54.2	200	mVolts
	732	3.8 Fan Status/Control				
	733	Set Initial Inputs to UUT for this test				
Pass	750	Measure HB_BUS (V)	-0.5	0.0094978	0.5	Vdc
Pass	753	Measure P28V_BUS (V)	-0.5	0.051458	0.5	Vdc
	754	Begin Test				
Pass	769	B.1 Measure P28V_BUS	27.8	27.997	28.2	Vdc
Pass	772	E.1 Verify RR(3) FAN_INHIBIT_IN = LOW	0	0	0	Bool
Pass	773	E.2 Verify RR(4) CV_INHIBIT_IN = LOW	0	0	0	Bool
Pass	775	G.1 Verify RR(10) FET_STATUS 0 = HIGH	1	1	1	Bool
Pass	776	G.2 Verify RR(10) FET_STATUS 1 = HIGH	1	1	1	Bool
Pass	777	G.3 Verify RR(10) PBIT_FLT_STS = 0	0	0	0	Bool
Pass	778	G.4 Verify P12V5 Voltage	12.2	12.51	12.8	Vdc
Pass	779	G.5 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	780	G.6 Verify RR(3) FAN_CURR_LMT = HIGH	1	1	1	Bool
Pass	781	G.7 Verify (RBW4) FAN_ON = HIGH	1	1	1	Bool
Pass	784	I.1 Verify FAN_PWR < 1V	-0.1	0.12964	1	Vdc
Pass	785	I.2 Verify RR(3) FAN_INHIBIT_IN = HIGH	1	1	1	Bool
Pass	786	I.3 Verify (RBW4) FAN_ON = LOW	0	0	0	Bool
Pass	787	I.4 Verify RR(3) FAN VOLTAGE LMT =LOW	0	0	0	Bool
Pass	788	I.4 Verify RR(3) FAN CURR LMT=LOW	0	0	0	Bool
Pass	790	K.1 Verify RR(3) FAN_ID = HIGH	1	1	1	Bool
Pass	791	K.2 Verify RR(3) FAN_INHIBIT_IN = LOW	0	0	0	Bool
Pass	793	K.3 Verify FAN_SPEED = F5 to FF (Hex)	245	249	255	Hz
Pass	796	M.1 Verify RR(3) FAN_ID = LOW	0	0	0	Bool
	798	3.9 FAN_INHIBIT_OUT				
	799	Set Initial Inputs to UUT for this test				
Pass	818	Measure HB_BUS (V)	-0.5	0.0084572	0.5	Vdc
	819	Set P28V_BUS				
Pass	821	Measure P28V_BUS	27.8	27.997	28.2	Vdc
	822	Begin Test				
Pass	832	B.1 Verify RR(3) FAN_INHIBIT_IN = LOW	0	0	0	Bool
Pass	833	B.2 Verify (RBW4) FAN_ON = LOW	0	0	0	Bool
Pass	834	C.1 Verify FAN_INHIBIT_OUT = ON	3.1	3.298	3.5	Vdc
Pass	836	E.1 Verify RR(3) FAN_INHIBIT_IN = LOW	0	0	0	Bool
Pass	837	E.2 Verify (RBW4) FAN_ON = LOW	0	0	0	Bool
Pass	839	F.1 Verify FAN_INHIBIT_OUT = OFF	-0.1	-0.0024924	0.1	Vdc
	840	3.10 Control Valve AUX Direction				
	841	Set Initial Inputs to UUT for this test				
Pass	860	Measure HB_BUS (V)	-0.5	0.0084743	0.5	Vdc
	861	Set P28V_BUS				
Pass	863	Measure P28V_BUS	27.8	27.998	28.2	Vdc
	864	Begin Test				
Pass	874	C.1 Verify RR(4) CV_POS = Binary 11	3	3	3	Decimal
Pass	930	G.1 Verify CV_PWR Voltage	-29.12	-27.926	-26.8	Vdc
Pass	931	G.2 Verify (RBW4) CV_ON_PIN=HIGH	1	1	1	Bool
Pass	932	G.3 Verify (RBW4) CV_DIR=LOW	0	0	0	Bool

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Status	Test	Test Description	Min		
Pass	308	K.3 Verify RR(7) MODULE_PRESENT_1	0		
Pass	309	K.4 Verify RR(7) MODULE_PRESENT_2	0		
Pass	310	K.5 Verify RR(7) MODULE_PRESENT_3	0		
Pass	311	K.6 Verify RR(7) MODULE_PRESENT_4	0		
Pass	312	K.7 Verify RR(7) MODULE_PRESENT_5	0		
Pass	313	K.8 Verify RR(7) MODULE_PRESENT_6	0		
Pass	314	K.9 Verify RR(7) MODULE_PRESENT_7	0		
Pass	315	K.10 Verify RR(6) MODULE_PRESENT_8	0		
Pass	316	K.11 Verify RR(6) MODULE_PRESENT_9	0		
Pass	317	K.12 Verify RR(6) MODULE_PRESENT_10	0		
Pass	318	K.13 Verify RR(6) MODULE_PRESENT_11	0		
Pass	319	K.14 Verify RR(6) MODULE_PRESENT_12	0		
Pass	320	K.15 Verify RR(6) MODULE_PRESENT_13	0		
Pass	321	K.16 Verify RR(6) MODULE_PRESENT_14	0		
Pass	322	K.17 Verify RR(4) CV_POS = MIDDLE	3		
	323	3.7 High-Line, No-Load Operation			
	324	Set Initial Inputs to UUT for this test			
Pass	341	Measure HB_BUS (V)	-0.5		
	343	Set P28V_BUS			
Pass	345	Measure P28V_BUS	35.8		
	346	Begin Test			
	364	A.1 Set all power outputs to NO LOAD			
Pass	371	B.1 Verify RR(1) P28V_LOCAL_LMT = HIGH	1		
Pass	372	B.2 Verify RR(1) P12V5_LMT = HIGH	1		
Pass	373	B.3 Verify P12V5 HL, NL	12.2		
Pass	374	B.4 Verify High line No-Load P12V5 ripple	10		
Pass	424	B.5 P12V5 Trans Neg	1	1	
Pass	474	B.6 P12V5 Trans Pulse	1	1	
Pass	524	B.7 P12V5 Trans Pos	1	1	
Pass	527	B.8 FAN_PWR Voltage	26.68	28.0	
Pass	528	B.9 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	
Pass	529	B.10 Verify RR(3) FAN_CURR_LMT = LOW	0	0	
Pass	534	D.1 Verify CV_PWR Voltage	-29.12	-28.0	
Pass	535	D.2 Verify RR(4) CV_VOLTAGE_LMT = HIGH	1	1	
Pass	536	D.3 Verify RR(4) CV_CURRENT_LMT = HIGH	1	1	
Pass	537	D.4 Verify P12V_BACKUP_OUT Voltage	11.52	11.94	1
Pass	539	D.5 Verify P12V_BACKUP_OUT Ripple	10	13.55	
Pass	542	E. Measure P28V_BUS	27.8	28	
Pass	545	F.1 Verify P28V_BUS Current	0.1	1.069	
Pass	546	F.2 Verify FAN_PWR Voltage	1	2.6021	
Pass	551	H. Measure P28V_BUS (V)	-0.5	0.053557	
	552	3.4 Power Monitors @ No Load			
	553	Set Initial Inputs to UUT for this test			
Pass	571	Measure HB_BUS (V)	35.8	36.005	
Pass	575	Measure P28V_BUS (V)	20	20.437	
	576	Begin Test			
	584	B. Set HB_BUS = 0V, then toggle P28V			
Pass	587	B. Measure HB_BUS (V)	-0.5	0.0099818	
Pass	590	B. Measure P28V_BUS (V)	-0.5	0.051057	
Pass	593	B. Measure P28V_BUS (V)	20	20.436	
Pass	596	D.1 Verify RR(1) P28V_LOCAL_LMT = HIGH	1	1	
Pass	597	D.2 Verify RR(1) P12V5_LMT = HIGH	1	1	

Status	Test	Test Description	Min.	Actual	Max.	Units
Pass	308	K.3 Verify RR(7) MODULE_PRESENT_1	0	0	0	Bool
Pass	309	K.4 Verify RR(7) MODULE_PRESENT_2	0	0	0	Bool
Pass	310	K.5 Verify RR(7) MODULE_PRESENT_3	0	0	0	Bool
Pass	311	K.6 Verify RR(7) MODULE_PRESENT_4	0	0	0	Bool
Pass	312	K.7 Verify RR(7) MODULE_PRESENT_5	0	0	0	Bool
Pass	313	K.8 Verify RR(7) MODULE_PRESENT_6	0	0	0	Bool
Pass	314	K.9 Verify RR(7) MODULE_PRESENT_7	0	0	0	Bool
Pass	315	K.10 Verify RR(6) MODULE_PRESENT_8	0	0	0	Bool
Pass	316	K.11 Verify RR(6) MODULE_PRESENT_9	0	0	0	Bool
Pass	317	K.12 Verify RR(6) MODULE_PRESENT_10	0	0	0	Bool
Pass	318	K.13 Verify RR(6) MODULE_PRESENT_11	0	0	0	Bool
Pass	319	K.14 Verify RR(6) MODULE_PRESENT_12	0	0	0	Bool
Pass	320	K.15 Verify RR(6) MODULE_PRESENT_13	0	0	0	Bool
Pass	321	K.16 Verify RR(6) MODULE_PRESENT_14	0	0	0	Bool
Pass	322	K.17 Verify RR(4) CV_POS = MIDDLE	3	3	3	Bool
	323	3.7 High-Line, No-Load Operation				
	324	Set Initial Inputs to UUT for this test				
Pass	341	Measure HB_BUS (V)	-0.5	0.011513	0.5	Vdc
	343	Set P28V_BUS				
Pass	345	Measure P28V_BUS	35.8	36	36.2	Vdc
	346	Begin Test				
	364	A.1 Set all power outputs to NO LOAD				
Pass	371	B.1 Verify RR(1) P28V_LOCAL_LMT = HIGH	1	1	1	Bool
Pass	372	B.2 Verify RR(1) P12V5_LMT = HIGH	1	1	1	Bool
Pass	373	B.3 Verify P12V5 HL, NL	12.2	12.51	12.8	Vdc
Pass	374	B.4 Verify High line No-Load P12V5 ripple	10	120	200	mVolts
Pass	424	B.5 P12V5 Trans Neg	1	1	1	Bool
Pass	474	B.6 P12V5 Trans Pulse	1	1	1	Bool
Pass	524	B.7 P12V5 Trans Pos	1	1	1	Bool
Pass	527	B.8 FAN_PWR Voltage	26.68	28.079	29.4	Vdc
Pass	528	B.9 Verify RR(3) FAN_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	529	B.10 Verify RR(3) FAN_CURR_LMT = LOW	0	0	0	Bool
Pass	534	D.1 Verify CV_PWR Voltage	-29.12	-28.091	-26.8	Vdc
Pass	535	D.2 Verify RR(4) CV_VOLTAGE_LMT = HIGH	1	1	1	Bool
Pass	536	D.3 Verify RR(4) CV_CURRENT_LMT = HIGH	1	1	1	Bool
Pass	537	D.4 Verify P12V_BACKUP_OUT Voltage	11.52	11.941	12.48	Vdc
Pass	539	D.5 Verify P12V_BACKUP_OUT Ripple	10	13.55	100	mVolts
Pass	542	E. Measure P28V_BUS	27.8	28	28.2	Vdc
Pass	545	F.1 Verify P28V_BUS Current	0.1	1.069	1.25	Adc
Pass	546	F.2 Verify FAN_PWR Voltage	1	2.6021	7	Vdc
Pass	551	H. Measure P28V_BUS (V)	-0.5	0.053557	0.5	Vdc
	552	3.4 Power Monitors @ No Load				
	553	Set Initial Inputs to UUT for this test				
Pass	571	Measure HB_BUS (V)	35.8	36.005	36.2	Vdc
Pass	575	Measure P28V_BUS (V)	20	20.437	21	Vdc
	576	Begin Test				
	584	B. Set HB_BUS = 0V, then toggle P28V				
Pass	587	B. Measure HB_BUS (V)	-0.5	0.0099818	0.5	Vdc
Pass	590	B. Measure P28V_BUS (V)	-0.5	0.051057	0.5	Vdc
Pass	593	B. Measure P28V_BUS (V)	20	20.436	21	Vdc
Pass	596	D.1 Verify RR(1) P28V_LOCAL_LMT = HIGH	1	1	1	Bool
Pass	597	D.2 Verify RR(1) P12V5_LMT = HIGH	1	1	1	Bool